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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,114	01/20/2004	Yoshiyuki Saito	50023-216	6651

7590 03/23/2006

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,114	SAITO ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 13 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchida et al. (US Patent 5,559,997).

2. As to claims 1, 13 and 16 Tsuchida discloses:

(1) A design-check system that checks electrical characteristics of CAD layout data for a printed circuit board, and comprising:

a storage means that stores position-specification conditions that specify a position from said CAD layout data where there is a possibility that poor electrical characteristics will occur due to an influence of CAD layout (a position to be evaluated, based on the layout information of the PC board-col.16, ll.18-20), characteristic-parameter items to be extracted, and correction-determination standards (The evaluation information storage unit 146 stores evaluation information. The evaluation information describes positions to be evaluated, ... and the evaluation rule for the positions –col.18, ll.55-58) that are standards for determining whether or not it is necessary to correct said CAD layout data, which are correlated and registered in a database for each predicted cause of poor electrical characteristics (The evaluation unit 131 performs a transmission line simulation by means of a well known method after the

layout unit 132 has completed a layout of the PC board. The evaluation unit 131 compares the output value of the evaluated position stored in the evaluation information storage unit 146 with the evaluation rule value, thereby evaluating whether the output value is within the evaluation rule. The transmission line simulation can be a cross talk simulation, electromagnetic radiation (EMI) simulation, timing simulation, or any combination of these simulations –col.16, ll.26-35) (Abstract; col.16, ll.18-59; col.18, ll.55-67; col.19, ll.1-44; col.21, ll.57-67; col.22, ll.1-13);

a position-specification means that specifies the position from said CAD layout data based on said position-specification conditions (The layout unit 132 performs a board layout including the placement of components and routing pattern, based on the component information- col.16, ll.60-63; the design rule generation unit 133 reads out circuit information ... (step 1101) -Fig.10; col.24, ll.32-36) (col.16, ll.60-67; col.17, ll.1-9; col.24, ll.32-36);

a characteristic-parameter-extraction means that is operable to extract said characteristic parameters based at said specified position (unit 133 also reads electrical and physical parameters of circuit/component- step 1101, Fig. 10; the reading is based on the information which indicates a target: "parallel route length L" in the design rule generation information, and information which indicates a parameter: "frequency of a signal to be transmitted, routing interval, dielectric constant of the board, width of routing foils, rising time in an output pin"- col.24, ll.55-60) (col.24, ll.26-67); and

a correction-determination means that to determines whether or not it is

necessary to correct said CAD layout data by comparing the characteristic parameters extracted by said characteristic-parameter-extraction means and said correction-determination standards that correspond to the characteristic parameters read from said storage means (The design rule generation unit 133 judges whether the bad influence such as cross talks to be caused between the parallel routes as a result of the simulation is within a negligible range or not, from the view point of the electric characteristics of the designed PC board. The judgment is done by seeing whether the output waveform of the position to be evaluated satisfies a predetermined evaluation rule) (col.25, ll.21-40; col.25, ll.65-67; col.26, ll.1-10);

(13) A program that is used in a design-check system that checks electrical characteristics of CAD layout data for a printed circuit board, and comprising (col.14, ll.1-12):

a storage means that stores position-specification conditions that specify a position from said CAD layout data where there is a possibility that poor electrical characteristics will occur due to an influence of CAD layout (a position to be evaluated, based on the layout information of the PC board-col.16, ll.18-20), characteristic-parameter items to be extracted, and correction-determination standards (The evaluation information storage unit 146 stores evaluation information. The evaluation information describes positions to be evaluated, ... and the evaluation rule for the positions –col.18, ll.55-58) that are standards for determining whether or not it is necessary to correct said CAD layout data, which are correlated and registered in a database for each predicted cause of poor electrical characteristics (The evaluation unit

131 performs a transmission line simulation by means of a well known method after the layout unit 132 has completed a layout of the PC board. The evaluation unit 131 compares the output value of the evaluated position stored in the evaluation information storage unit 146 with the evaluation rule value, thereby evaluating whether the output value is within the evaluation rule. The transmission line simulation can be a cross talk simulation, electromagnetic radiation (EMI) simulation, timing simulation, or any combination of these simulations –col.16, ll.26-35) (Abstract; col.16, ll.18-59; col.18, ll.55-67; col.19, ll.1-44; col.21, ll.57-67; col.22, ll.1-13);

a position-specification means that specifies the position from said CAD layout data based on said position-specification conditions (The layout unit 132 performs a board layout including the placement of components and routing pattern, based on the component information- col.16, ll.60-63; the design rule generation unit 133 reads out circuit information ... (step 1101) -Fig.10; col.24, ll.32-36) (col.16, ll.60-67; col.17, ll.1-9; col.24, ll.32-36);

a characteristic-parameter-extraction means that is operable to extract said characteristic parameters based at said specified position (unit 133 also reads electrical and physical parameters of circuit/component- step 1101, Fig. 10; the reading is based on the information which indicates a target: "parallel route length L" in the design rule generation information, and information which indicates a parameter: "frequency of a signal to be transmitted, routing interval, dielectric constant of the board, width of routing foils, rising time in an output pin"- col.24, ll.55-60) (col.24, ll.26-67); and

a correction-determination means that to determines whether or not it is

necessary to correct said CAD layout data by comparing the characteristic parameters extracted by said characteristic-parameter-extraction means and said correction-determination standards that correspond to the characteristic parameters read from said storage means (The design rule generation unit 133 judges whether the bad influence such as cross talks to be caused between the parallel routes as a result of the simulation is within a negligible range or not, from the view point of the electric characteristics of the designed PC board. The judgment is done by seeing whether the output waveform of the position to be evaluated satisfies a predetermined evaluation rule) (col.25, ll.21-40; col.25, ll.65-67; col.26, ll.1-10) ;

(16) A design-check methd that checks electrical characteristics of CAD layout data for a printed circuit board, and comprising (col.13, ll.65-67):

a storage means that stores position-specification conditions that specify a position from said CAD layout data where there is a possibility that poor electrical characteristics will occur due to an influence of CAD layout (a position to be evaluated, based on the layout information of the PC board-col.16, ll.18-20), characteristic-parameter items to be extracted, and correction-determination standards (The evaluation information storage unit 146 stores evaluation information. The evaluation information describes positions to be evaluated, ... and the evaluation rule for the positions –col.18, ll.55-58) that are standards for determining whether or not it is necessary to correct said CAD layout data, which are correlated and registered in a database for each predicted cause of poor electrical characteristics (The evaluation unit 131 performs a transmission line simulation by means of a well known method after the

layout unit 132 has completed a layout of the PC board. The evaluation unit 131 compares the output value of the evaluated position stored in the evaluation information storage unit 146 with the evaluation rule value, thereby evaluating whether the output value is within the evaluation rule. The transmission line simulation can be a cross talk simulation, electromagnetic radiation (EMI) simulation, timing simulation, or any combination of these simulations –col.16, ll.26-35) (Abstract; col.16, ll.18-59; col.18, ll.55-67; col.19, ll.1-44; col.21, ll.57-67; col.22, ll.1-13);

a position-specification means that specifies the position from said CAD layout data based on said position-specification conditions (The layout unit 132 performs a board layout including the placement of components and routing pattern, based on the component information- col.16, ll.60-63; the design rule generation unit 133 reads out circuit information ... (step 1101) -Fig.10; col.24, ll.32-36) (col.16, ll.60-67; col.17, ll.1-9; col.24, ll.32-36);

a characteristic-parameter-extraction means that is operable to extract said characteristic parameters based at said specified position (unit 133 also reads electrical and physical parameters of circuit/component- step 1101, Fig. 10; the reading is based on the information which indicates a target: "parallel route length L" in the design rule generation information, and information which indicates a parameter: "frequency of a signal to be transmitted, routing interval, dielectric constant of the board, width of routing foils, rising time in an output pin"- col.24, ll.55-60) (col.24, ll.26-67); and

a correction-determination means that to determines whether or not it is

necessary to correct said CAD layout data by comparing the characteristic parameters extracted by said characteristic-parameter-extraction means and said correction-determination standards that correspond to the characteristic parameters read from said storage means (The design rule generation unit 133 judges whether the bad influence such as cross talks to be caused between the parallel routes as a result of the simulation is within a negligible range or not, from the view point of the electric characteristics of the designed PC board. The judgment is done by seeing whether the output waveform of the position to be evaluated satisfies a predetermined evaluation rule) (col.25, ll.21-40; col.25, ll.65-67; col.26, ll.1-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11, 12, 2-10, 14-15 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable by Tsuchida in view of Hara et al. (US Pub. No.: 20030097246.

4. As to claims 11, 12 and 17 Tsuchida discloses:

(11) An apparatus that is used in a design-check system and checks the electrical characteristics of CAD layout data for a printed circuit board, and comprises:

a storage means that stores position-specification conditions that specify a position from said CAD layout data where there is a possibility that poor electrical

characteristics will occur due to an influence of the CAD layout, characteristic-parameter items to be extracted at the specified position, and correction-determination standards that are standards for determining whether or not it is necessary to correct the CAD layout data, which are correlated and registered in a database for each predicted cause of the poor electrical characteristics (Abstract; col.16, ll.18-59; col.18, ll.55-67; col.19, ll.1-44; col.21, ll.57-67; col.22, ll.1-13); and

a correction-determination means that receives the characteristic parameters that were extracted by the apparatus for a position specified from the input CAD layout data based on said position-specification conditions, and determines whether or not it is necessary to correct the CAD layout by comparing the characteristic parameters with correction-determination standards that correspond to the characteristic parameters read from said storage means, and then sends the determination result to said apparatus (col.16, ll.60-67; col.17, ll.1-9; col.24, ll.26-67; col.25, ll.21-40; col.25, ll.65-67; col.26, ll.1-10);

(12) An apparatus that is used in a design-check system and that uses CAD layout data for a printed circuit board, apparatus comprising:

a position-specification means that specifies a position from said CAD layout data based on position-specification conditions that specifies the position where there is a possibility of the occurrence of poor electrical characteristics due to an influence of CAD layout (Abstract; col.16, ll.18-59; col.16, ll.60-67; col.17, ll.1-9; col.18, ll.55-67; col.19, ll.1-44; col.21, ll.57-67; col.22, ll.1-13; col.24, ll.32-36) ; and

a characteristic-parameter-extraction means that extracts characteristic parameters at said specified position, and sends those characteristic parameters to said apparatus (col.24, ll.26-67);

(17) A design-check method whereby checks electrical characteristics of CAD layout data for a printed circuit board input, the method comprising:

a step of specifying a position from said CAD layout data based on position-specification conditions that specify the position where there is a

possibility of poor electrical characteristics due to an influence of CAD layout (col.16, ll.60-67; col.17, ll.1-9; col.24, ll.32-36);

a step of extracting characteristic parameters at the specified position (col.24, ll.26-67);

a step wherein apparatus reads correction-determination standards that correspond to said characteristic parameters from the database in which said position-specification conditions, characteristic-parameter items to be extracted, and correction-determination standards, which are standards for determining whether or not it is necessary to correct the CAD layout data, are correlated and registered (Abstract; col.16, ll.18-59; col.18, ll.55-67; col.19, ll.1-44; col.21, ll.57-67; col.22, ll.1-13); and

a step wherein said apparatus compares characteristic parameters and correction-determination standards read from said database, and determines whether or not it is necessary to correct the CAD layout data (col.25, ll.21-40; col.25, ll.65-67; col.26, ll.1-10).

With respect to claims 11, 12 and 17 Tsuchida teaches the features above but lacks an apparatus/method for checking electrical characteristics of CAD layout data for a printed circuit board, wherein design-check system includes a server and a client interfaced by an internet.

As to claims 11, 12 and 17 Hara recites:

an apparatus/method for checking electrical characteristics of CAD layout data for a printed circuit board, wherein design-check system includes a server and a client interfaced by an internet (Abstract; [0004]; [0032]- [0033]; [0041]- [0043]).

5. As to claims 2-10, 14-15 and 18-19 Hara recites:

an apparatus/method for checking electrical characteristics of CAD layout data for a printed circuit board, wherein design-check system includes a server and a client interfaced by an internet and server further comprises billing information (Abstract; [0004]; [0032]- [0033]; [0041]- [0043]).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Hara's teaching regarding the apparatus/method for checking electrical characteristics of CAD layout data for a printed circuit board, wherein design-check system includes a server and a client interfaced by an internet and use it in Tsuchida's invention to provide the apparatus/method, in which leakage of confidential technical information on internal circuits of printed circuit boards can be prevented while supplying results of high-accuracy calculation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

THUAN DO
Primary examiner
03/08/06